WHAT IS CLAIMED IS:

1. A measuring apparatus for measuring jitter transfer function of an electronic device, comprising:

a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output from said electronic device; and

a jitter transfer function estimator operable to calculate jitter transfer function of said electronic device based on said output timing jitter sequence.

2. A measuring apparatus as claimed in claim 1, wherein said timing jitter estimator comprises:

an instantaneous phase noise estimator operable to calculate an instantaneous phase noise of said output signal based on said output signal; and

a resampler operable to generate said output timing jitter sequence obtained by resampling said instantaneous phase noise at predetermined timings.

3. A measuring apparatus as claimed in claim 2, wherein said resampler resamples said instantaneous phase noise at timings approximately same as zero-crossing timings of said output signal.

4. A measuring apparatus as claimed in claim 1, wherein said electronic device receives a plurality of input signals having different jitter amounts and outputs said plurality of output signals respectively corresponding to said plurality of input signals,

said timing jitter estimator calculates said output timing jitter sequences corresponding to said output signals respectively, and

said jitter transfer function estimator calculates said jitter transfer function further based on said information indicating a plurality of input timing jitter sequences corresponding to said plurality of input signals.

5. A measuring apparatus as claimed in claim 1, wherein said electronic device receives a plurality of input signals having different jitter amounts one after another and outputs a plurality of said output signals respectively corresponding to said input signals,

said timing jitter estimator receives said plurality of input signals one after another and calculates a plurality of input timing jitter sequences of said plurality of input signals, and receives said plurality of output signals one after another and calculates said output timing jitter sequences of said output signals respectively, and

said jitter transfer function estimator calculates said jitter transfer function further based on said input timing jitter sequences.

6. A measuring apparatus as claimed in claim 4 or 5, further comprising a frequency-domain transformer operable to transform said input timing jitter sequences and said output timing jitter sequences to frequency domain signals.

7. A measuring apparatus claimed in claim 6, wherein said jitter transfer function estimator comprises a jitter gain

estimator operable to calculate a gain $|H_J(f_J)|$ of said jitter transfer function based on the following Equation:

$$|H_J(f_J)| = \left|\frac{\Delta\Phi[f_J]}{\Delta\Theta[f_J]}\right| \quad or \quad |H_J(f_J)| = \left|\frac{\Delta\Phi(f_J)}{\Delta\Theta(f_J)}\right|$$

where $\Delta\Phi[f_J]$ is an output timing jitter spectra of the output signal; $\Delta\Theta[f_J]$ is an input timing jitter spectra of the input signal; $\Delta\Phi(f_J)$ is a phase noise spectra of the output signal; and $\Delta\Theta(f_J)$ is a phase noise spectra of the input signal.

8. A measuring apparatus as claimed in claim 5, wherein said jitter transfer function estimator comprises a jitter gain estimator operable to calculate a gain of said jitter transfer function based on said plurality of input timing jitter sequences and said plurality of output timing jitter sequences.

9. A measuring apparatus as claimed in claim 8, wherein said jitter gain estimator calculates said gain of said jitter transfer function based on a result of linear fitting of a relationship between a peak-to-peak value of an input timing jitter of said plurality of input timing jitter sequences and a peak-to-peak value of an output timing jitter of said plurality of output timing jitter sequences, or a root-mean-square (RMS) value of said output timing jitter of said output timing jitter sequences and a root-mean-square value of an input timing jitter of said plurality of input timing jitter sequences.

10. A measuring apparatus as claimed in claim 6, wherein said jitter transfer function estimator comprises a jitter phase estimator operable to calculate a phase $\angle H_J(f_J)$ of said jitter transfer function based on the following Equation:

$$\angle H_J(f_J) = \tan^{-1}\frac{\mathrm{Im}[H_J(f_J)]}{\mathrm{Re}[H_J(f_J)]}$$

where $\Delta\Phi[f_J]$ is an output timing jitter spectra of the output signal; $\Delta\Theta[f_J]$ is an input timing jitter spectra of the input signal; $\Delta\Phi(f_J)$ is a phase noise spectra of the output signal; and $\Delta\Theta(f_J)$ is a phase noise spectra of the input signal.

11. A measuring apparatus as claimed in claim 5 or 8, further comprising a jitter applying unit operable to supply a signal, which is obtained by applying said desired input timing jitter to said input signal, to said electronic device,

wherein said jitter gain estimator estimates said gain of said jitter transfer function based on said input timing jitter applied to said input signal by said jitter applying unit and said output timing jitter in said output signal.

12. A measuring apparatus as claimed in claim 11, wherein said jitter applying unit applies a sinusoidal jitter to said input signal as said input timing jitter.

13. A measuring apparatus as claimed in claim 12, wherein said jitter applying unit applies said input timing jitter by modulating a phase of said input signal.

14. A measuring apparatus as claimed in claim 12, wherein said jitter applying unit applies said input timing jitter by modulating a frequency of said input signal.

15. A measuring apparatus as claimed in claim 1, further comprising a clock recovery unit operable to generate a recovered clock signal of said output signal based on said output signal,

wherein said timing jitter estimator estimates said output timing jitter based on said recovered clock signal.

16. A measuring apparatus as claimed in claim 2, wherein said instantaneous phase noise estimator comprise:

an analytic signal transformer operable to transform said output signal to a complex analytic signal;

an instantaneous phase estimator operable to estimate an instantaneous phase of said analytic signal based on said analytic signal;

a linear instantaneous phase estimator operable to estimate a linear instantaneous phase of said output signal based on an instantaneous phase of said analytic signal; and

a linear trend remover operable to calculate an instantaneous phase noise obtained by removing said linear instantaneous phase from said instantaneous phase based on said instantaneous phase and said linear instantaneous phase.

17. A measuring apparatus as claimed in claim 16, wherein said timing jitter estimator further comprises a low frequency phase noise remover operable to receive said instantaneous phase noise, removes low frequency components of said instantaneous phase noise and supplies said instantaneous phase noise with no low frequency component to said resampler.

18. A measuring apparatus as claimed in claim 16, wherein said timing jitter estimator further comprises an analog-to-digital converter operable to convert said output signal to a digital signal and supplies said digital signal to said analytic signal transformer,

wherein said analytic signal transformer generates said analytic signal based on said digital signal.

19. A measuring apparatus as claimed in claim 1, wherein said timing jitter estimator estimates a timing jitter sequence of input data clock signal for generating input data signal given to said electronic device, and a timing jitter sequence of output data signal output from said electronic device in response to said input data signal, and

said jitter transfer function measuring apparatus measures jitter transfer function between said input data clock signal and said output data signal based on said timing jitter sequence estimated by said timing jitter estimator.

20. A measuring apparatus as claimed in claim 1, wherein said timing jitter estimator estimates a timing jitter sequence of an input data signal given to said electronic device and an output data signal output from said electronic device in response to said input data signal, and

said jitter transfer function measuring apparatus measures a jitter transfer function between said input data signal and said output data signal based on said timing jitter sequence estimated by said timing jitter estimator.

21. A measuring apparatus as claimed in claim 1, wherein said timing jitter estimator estimates timing jitter sequence of input data signal given to said electronic device and recovered clock signal output from said electronic device in response to said input data, and

said jitter transfer function measuring apparatus measures a jitter transfer function between said input data

signal and said recovered clock signal based on said timing jitter sequence estimated by said timing jitter estimator.

22. A measuring apparatus as claimed in claim 1, wherein

said timing jitter estimator estimates a timing jitter sequence of an input data clock signal for generating the input data signal given to said electronic device, and a recovered clock signal output from said electronic device in response to said input data, and

said jitter transfer function measuring apparatus measures a jitter transfer function between said input data clock signal and said recovered clock signal based on said timing jitter sequence estimated by said timing jitter estimator.

23. A measuring apparatus as claimed in any of claims 19-22, wherein

said electronic device receives serial data as said input data signal, and outputs a parallel data as said output data signal from output pins, the number of output pins being predetermined,

said timing jitter estimator estimates said output timing jitter sequence of said output data signal according to data output from a certain output pin out of said output pins, and

said input unit supplies said input data signal to said electronic device, in which a bit of the pattern data corresponding to the certain output pin out of said output pins repeats 1 (high) and 0 (low) by turns.

24. A measuring apparatus as claimed in claim 23, wherein

said input unit supplies said input data signal to said electronic device, in which bits of the pattern data repeats 1 and 0 every bits same number as said output pins.

25. A measuring apparatus for measuring a bit error rate of an electronic device, comprising a bit error rate estimator operable to estimate said bit error rate of said electronic device based on a gain of jitter transfer function of said electronic device.

26. A measuring apparatus as claimed in claim 25, wherein said bit error rate estimator estimates said bit error rate further based on a phase of said jitter transfer function.

27. A measuring apparatus for measuring jitter tolerance of an electronic device, comprising a jitter tolerance estimator operable to estimate said jitter tolerance of said electronic device based on a gain of jitter transfer function of said electronic device.

28. A measuring apparatus as claimed in claim 27, wherein said jitter tolerance estimator estimates said jitter tolerance further based on a phase of said jitter transfer function.

29. A measuring apparatus as claimed in claim 27 or 28, wherein

said jitter tolerance estimator estimates a coarse value of the jitter tolerance based on the gain estimate of the jitter transfer function, and

the measuring apparatus further comprises

a signal input means operable to input into the electronic device the plurality of input signals to which timing jitter

having different amplitudes in the vicinity of an amplitude value in accordance with the coarse value of the jitter tolerance are applied one after another, and

a bit error detector operable to detect bit error in the output signal by comparing each bit of a reference signal, which the electronic device is to output in response to the input signal to which the timing jitter is applied, with each bit of the output signal which the electronic device outputs in accordance with the input signal, and

said jitter tolerance estimator estimates peak-to-peak value of the input timing jitter, above which said bit error detector starts to detect the bit error in the output signal, the input timing jitter corresponding to the jitter tolerance.

30. The measuring apparatus as claimed in claim 29, wherein

said bit error detector samples data signal output from the electronic device at the edge of the clock signal output from the electronic device, converts the data signal into a logic valued sequence (data sequence), and compares each bit of the detected data sequence with each bit of the given reference pattern signal.

31. A measuring apparatus as claimed in claim 27 or 28, further comprising:

a jitter applying unit operable to supply a first check signal, to which a timing jitter is applied, to said electronic device, the timing jitter having amplitude according to said jitter tolerance estimated by said jitter tolerance estimator;

a jitter distortion estimator operable to estimate jitter distortion of an output timing jitter of said output signal output from said electronic device according to said first check signal,

against an ideal timing jitter of said output signal which said electronic device is to output according to said first check signal; and

a judging unit operable to judge whether said jitter tolerance is a right value based on said jitter distortion.

32. A measuring apparatus as claimed in claim 31, wherein when said judging unit judges that said jitter tolerance estimated by said jitter tolerance estimator is not a right value,

said jitter applying unit supplies a second check signal, to which a timing jitter is applied, to said electronic device, the timing jitter having smaller amplitude than said first check signal,

said jitter distortion estimator estimates jitter distortion of an output timing jitter of said output signal output from said electronic device according to said second check signal, against an ideal timing jitter of said output signal which said electronic device is to output according to said second check signal, and

said judging unit newly estimates said jitter tolerance based on said jitter distortion, estimated by said jitter distortion estimator, and corresponding to said second check signal.

33. A measuring apparatus for measuring a bit error rate of an electronic device, comprising:

a timing estimator operable to estimate an input timing sequence of an input signal for testing said electronic device and an output timing sequence of an output signal output from said electronic device in response to said input signal;

a timing difference estimator operable to calculate timing differences between said input timing sequence and said output timing sequence; and

a bit error rate estimator operable to estimate said bit error rate of said electronic device based on said timing differences.

34. A measuring apparatus as claimed in claim 33, wherein said timing estimator estimates said input timing sequence and said output timing sequence based on a zero-crossing timing sequence of rising edges or falling edges of said input signal and said output signal.

35. A measuring apparatus as claimed in claim 33, wherein said timing estimator comprises:

an analytic signal transformer operable to transform said input signal and said output signal into complex analytic signals;

an instantaneous phase estimator operable to calculate instantaneous phases of said analytic signals; and

a resampler operable to resample said instantaneous phase to generate timing sequences of said input signal and said output signal.

36. A measuring method for measuring jitter transfer function of an electronic device, comprising:

a timing jitter estimation step of calculating an output timing jitter sequence, which indicates a plurality of output timing jitter of an output signal, based on said output signal output from said electronic device; and

a jitter transfer function estimation step of calculating jitter transfer function of said electronic device based on said output timing jitter sequence.

37. A measuring method for measuring a bit error rate of an electronic device, comprising a bit error rate estimation step of estimating said bit error rate of said electronic device based on a gain of jitter transfer function of said electronic device.

38. A measuring method for measuring jitter tolerance of an electronic device, comprising a jitter tolerance estimation step of estimating said jitter tolerance of said electronic device based on a gain of jitter transfer function of said electronic device.

39. A measuring method for measuring a bit error rate of an electronic device, comprising:

estimating an input timing sequence of an input signal for testing said electronic device and an output timing sequence of an output signal output from said electronic device in response to said input signal;

calculating timing differences between said input timing sequence and said output timing sequence; and

estimating said bit error rate of said electronic device based on said timing differences.

40. A measuring apparatus for measuring reliability of an electronic device against jitter, comprising:

a timing jitter estimator operable to estimate an output timing jitter sequence of an output signal based on said output

signal output from said electronic device in response to an input signal to which an input timing jitter is applied;

a jitter distortion estimator operable to estimate jitter distortion of an output timing jitter of said output signal output from said electronic device in response to said input signal, against an ideal timing jitter of said output signal which said electronic device is to output in response to said input signal based on said output timing jitter sequence; and

a jitter related transmission penalty estimator operable to estimate said reliability of said electronic device against jitter based on said jitter distortion.

41. A measuring apparatus as claimed in claim 40, further comprising a jitter applying unit operable to apply said input timing jitter, having a desired amplitude, to said input signal, and to supply said input signal to said electronic device, wherein

said jitter related transmission penalty estimator estimates said reliability of said electronic device against jitter about amplitude of said input timing jitter.

42. A measuring apparatus as claimed in claim 41, wherein

said jitter applying unit supplies said plurality of input signals, having different amplitudes of said input timing jitter, to said electronic device, and

said jitter related transmission penalty estimator estimates jitter tolerance of said electronic device based on jitter distortion of each of said output timing jitter against said plurality of input signals.

43. A measuring apparatus as claimed in claim 40, wherein

said jitter tolerance estimator estimates a coarse value of the jitter tolerance based on jitter distortion of the output timing jitter, and

the measuring apparatus further comprises

a signal input means operable to input into the electronic device the input signals to which timing jitter having different amplitudes in the vicinity of an amplitude value in accordance with the coarse value of the jitter tolerance are applied one after another, and

a bit error detector operable to detect bit error in the output signal by comparing each bit of a reference pattern signal, which the electronic device is to output in response to the input signal to which the timing jitter is applied, with each bit of the output signal which the electronic device outputs in accordance with the input signal, and

said jitter tolerance estimator estimates peak-to-peak value of the input timing jitter, above which said bit error detector starts to detect the bit error in the output signal, the input timing jitter corresponding to the jitter tolerance.

44. A measuring apparatus as claimed in claim 42, further comprising

a signal input means operable to apply an input timing jitter to the input signal and

a bit error detector operable to detect bit error in the output signal by comparing each bit of a reference pattern signal, which the electronic device is to output in response to the input signal to which the timing jitter is applied, with each bit of the output signal which the electronic device outputs in accordance with the input signal, and

said jitter related transmission penalty estimator selectively changes an amplitude of the input timing jitter until said bit error detector detects the bit error, and estimates peak-to-peak value of the input timing jitter, above which said bit error detector starts to detect the bit error, the input timing jitter giving the jitter tolerance, or selectively calculates the jitter tolerance based on the jitter distortion of the output timing jitter.

45. The measuring apparatus as claimed in claim 44, wherein

said bit error detector samples data signal output from the electronic device at the edge of the clock signal output from the electronic device, converts the data signal into a logic valued sequence (data sequence), and compares each bit of the detected data sequence with each bit of the given reference pattern signal.

46. A measuring apparatus as claimed in claim 41 or 42, wherein

said jitter applying unit applies a sinusoidal jitter to said input signal, and

said jitter distortion estimator generates a jitter histogram of said output timing jitter sequence, and calculates jitter distortion of said output timing jitter based on said jitter histogram.

47. A measuring apparatus as claimed in claim 41 or 42, wherein

said jitter applying unit applies a sinusoidal jitter to said input signal, and

said jitter distortion estimator estimates a jitter spectrum of said output timing jitter sequence, and calculates

jitter distortion of said output timing jitter based on said jitter spectrum.

48. A measuring apparatus as claimed in claim 47, wherein said jitter distortion estimator estimates jitter distortion of said output timing jitter based on ratio of fundamental frequency content of said jitter spectrum, having the same frequency as said sinusoidal jitter, and harmonic content of said fundamental frequency content in said jitter spectrum.

49. A measuring apparatus as claimed in claim 42, wherein

said jitter distortion estimator estimates amplitude of said output timing jitter against said plurality of sinusoidal jitters having different amplitude, and

said jitter related transmission penalty estimator estimates said jitter tolerance based on amplitude of said sinusoidal jitter, where the amplitude of said output timing jitter, in response to amplitude of said sinusoidal jitter, becomes nonlinear.

50. A measuring apparatus as claimed in claim 41, wherein

said jitter applying unit supplies said input signal to said electronic device, where said plurality of sinusoidal jitters having different frequency are applied to said input signal, and

said jitter related transmission penalty estimator estimates said reliability of said electronic device against jitter about every frequency of said sinusoidal jitter.

51. A measuring apparatus as claimed in claim 1 or 40, wherein said timing jitter estimator comprises:

a period jitter estimator operable to estimate period jitter sequence of said output signal;

an ideal edge timing estimator operable to estimate average period of said period jitter sequence; and

an edge timing error estimation unit operable to estimate said output timing jitter sequence based on said average period of said period jitter sequence and said period jitter sequence.

52. A measuring method for measuring reliability of an electronic device against jitter, comprising:

a timing jitter estimation step for estimating an output timing jitter sequence of an output signal based on said output signal output from said electronic device in response to an input signal to which an input timing jitter is applied;

a jitter distortion estimation step for estimating jitter distortion of an output timing jitter of said output signal output from said electronic device in response to said input signal, against an ideal timing jitter of said output signal which said electronic device is to output in response to said input signal based on said output timing jitter sequence; and

a jitter related transmission penalty estimation step for estimating said reliability of said electronic device against jitter based on said jitter distortion.

53. A measuring apparatus for measuring jitter transfer function of an electronic device, comprising:

a timing jitter estimator operable to estimate an output instantaneous phase noise of said output signal based on an output signal output from said electronic device; and

a jitter transfer function measuring apparatus operable to measure a jitter transfer function in said electronic device based on said output instantaneous phase noise.